IN THE SPECIFICATION:

1. Please replace page 1 with the following text:

A MULTIMODE DECODER

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of United Kingdom patent application no. 0328794.3. and PCT Application PCT/IB2004/004349 filed 12/13/2004.

FIELD OF THE INVENTION

The present invention relates to a decoder.

BACKGROUND OF THE INVENTION

Wireless communication systems are widely deployed to provide various types of communications such as voice and data. One such system is wideband code division multiple access WCDMA, which has been adopted in various competing wireless communication standards, for example 3rd generation partnership project 3GPP and 3GPP2.

To overcome data corruption that can occur during RF transmission the different wireless communication standards typically include some form of channel coding. For example, WCDMA standards typically require that a WCDMA receiver decode a mixture of turbo encoded and viterbi encoded data streams, where viterbi encoded channels are typically used for time critical data.

In particular the 3GPP standard has specified a high speed data packed access HSDPA sub-system that has two physical channels in the downlink direction; a data channel and a control channel in which turbo coding is used to encode the data channel and convolutional coding is used to encode the control channel.

A turbo encoder uses a first convolutional encoder to encode information bits (i.e. systematic bits) within a packet to generate a first sequence of parity bits (i.e. parity 1 bits) in parallel to the interleaver shuffling the information bits, where the shuffled information bits are encoded by a second encoder to generate a second sequence of parity bits (i.e. parity 2 bits). The information bits and the parity bits in the first and second sequence are then modulated and transmitted to a receiver.

2. Please replace page 3 with the following text:

The basic transmission unit in a HSDPA sub-system is called a time transmission interval TTI where each TTI spans 2ms and contains three identical time periods called slots.

As shown in figure 1, for each TTI transmitted in the data channel 100 there is a corresponding TTI in the control channel 200 that starts 2 slots before the beginning of the associated data channel TTI.

The control data is divided into two parts. The first part 102, which contains information required for the demodulation of the corresponding data channel TTI, is transmitted in the first slot of the control channel TTI. The second part 103, which contains data required for the channel decoding of the corresponding data channel TTI, is transmitted in the second and third slots of the control channel TTI.

There is a period of one slot to decode the first part of the control channel before the decoded data is required for the demodulation of the data channel. Similarly, there is a two slot period to decode the second part of the control channel before the decoded data is required for decoding of the data channel. This arrangement results in severe timing restrictions on the decoding of the control channel part.

One solution to this problem has been the use of a separate turbo decoder for decoding the turbo encoded channels and a separate viterbi decoder for decoding the convolutional encoded channels; however this results in increased cost and size of a receiver.

It is desirable to improve this situation.

BRIEF SUMMARY OF THE INVENTION

In accordance with a first aspect of the present invention there is provided a decoder according to claim 1.

3. Please replace page 4 with the following text:

This provides the advantage of allowing a single decoder to support the decoding of a turbo encoded channel and a convolutional encoded channel.

BRIEF DESCRIPTION OF THE DRAWINGS

An embodiment of the invention will now be described, by way of example, with reference to the drawings, in which:

Figure 1 illustrates the structure of a known HS-DPA data channel and control channel;

Figure 2 illustrates a WCDMA receiver according to an embodiment of the present invention;

Figure 3 illustrates a decoder according to an embodiment of the present invention;

Figure 4 illustrates a first memory structure according to an embodiment of the present invention;

Figure 5 illustrates a second memory structure according to an embodiment of the present invention.

DESCRIPTION OF PREFERRED EMBODIMENT(S)

Figure 2 shows a WCDMA receiver 200 having a memory module 201 (e.g. a buffer), a controller 202 and a decoder 203.

The memory module 201 has a first input for receiving encoded data, a second input for receiving decoded data from the decoder 203, a first output for outputting decoded data, and a second output for providing stored data to the